

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : H. OHTANI  
Serial No.: 08/730,038  
Filed : 5/23/97  
Title : SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATING METHOD  
THEREOF

Art Unit:  
Examiner:

Assistant Commissioner for Patents  
Washington, DC 20231

TRANSMITTAL OF PRIORITY DOCUMENT(S) UNDER 35 U.S.C. 119

Applicant hereby confirms his claim of priority under 35 U.S.C. 119 from Japanese Application No. 8-165272 filed June 4, 1996. A certified copy of the application from which priority is claimed is submitted herewith.

Please charge any fees due in this respect to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/15/97

  
\_\_\_\_\_  
Scott C. Harris  
Reg. No. 32,030

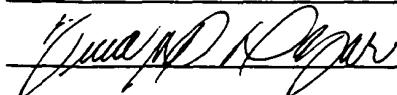
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36106.LJ1

Date of Deposit 7-16-97  
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

YINIA M. NAJAR



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別紙添付の書類に記載されている事項は下記の出願書類に記載されて  
る事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed  
in this Office.

出願年月日  
Date of Application: 1996年 6月 4日

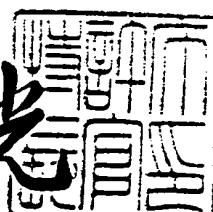
出願番号  
Application Number: 平成 8年特許願第165272号

出願人  
Applicant(s): 株式会社半導体エネルギー研究所

1997年 5月16日

特許庁長官  
Commissioner,  
Patent Office

荒井寿考



出証番号 出証特平09-3035926